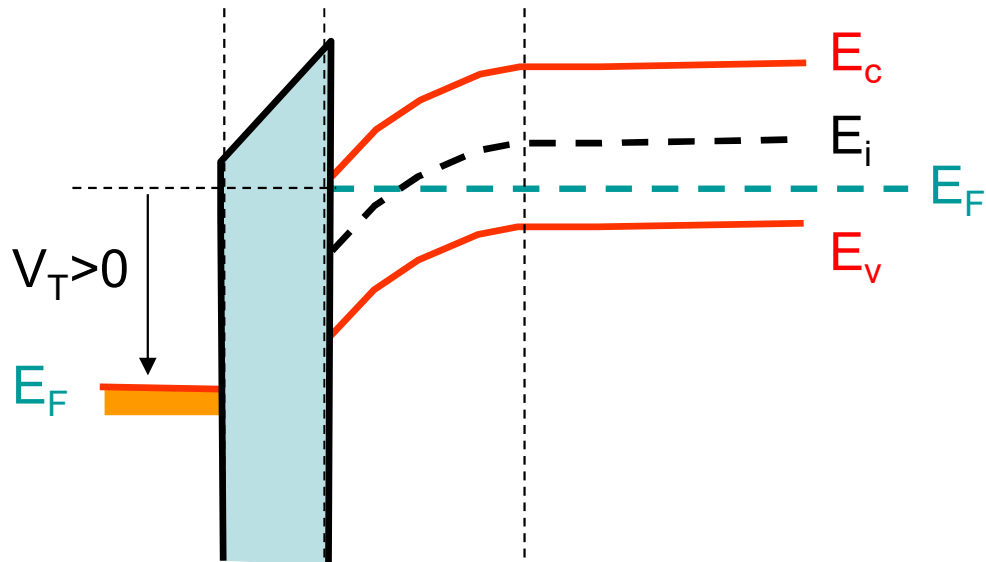
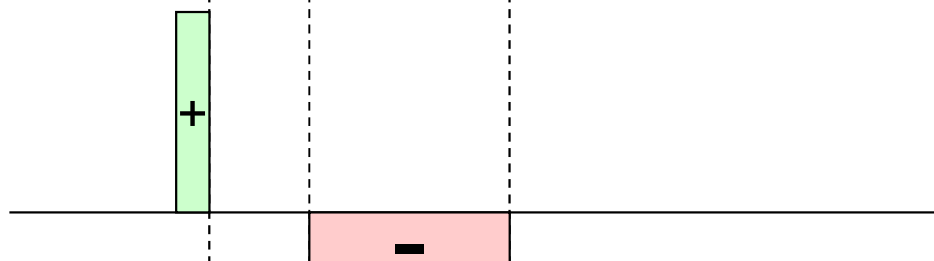


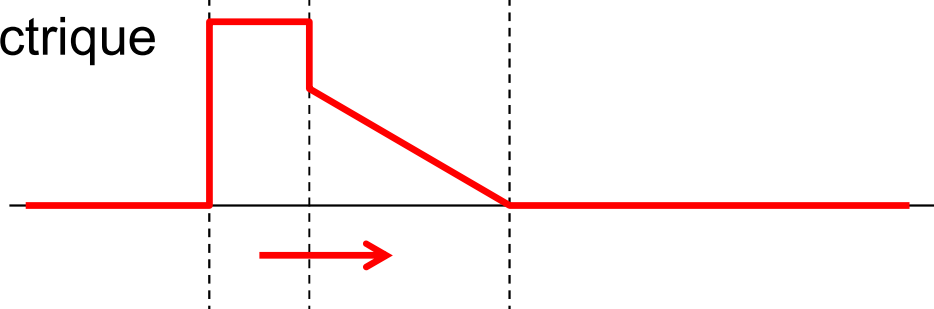
Bandes



Charges



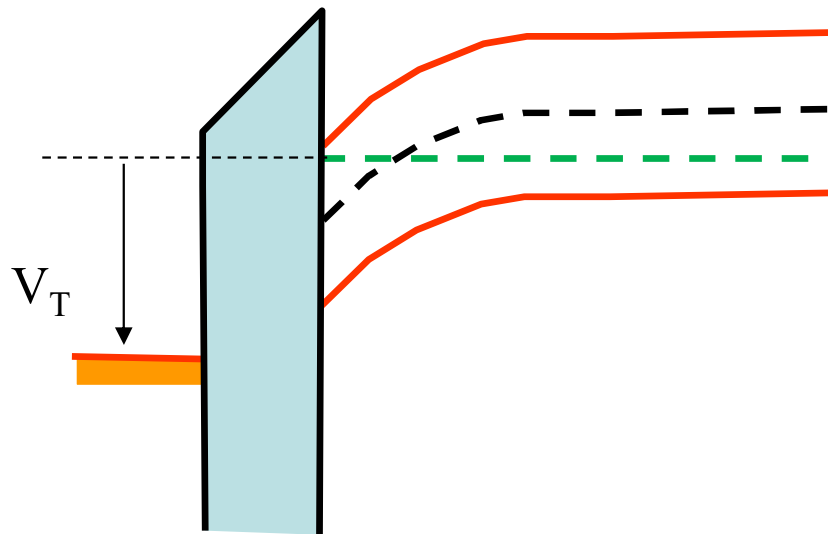
Champ électrique



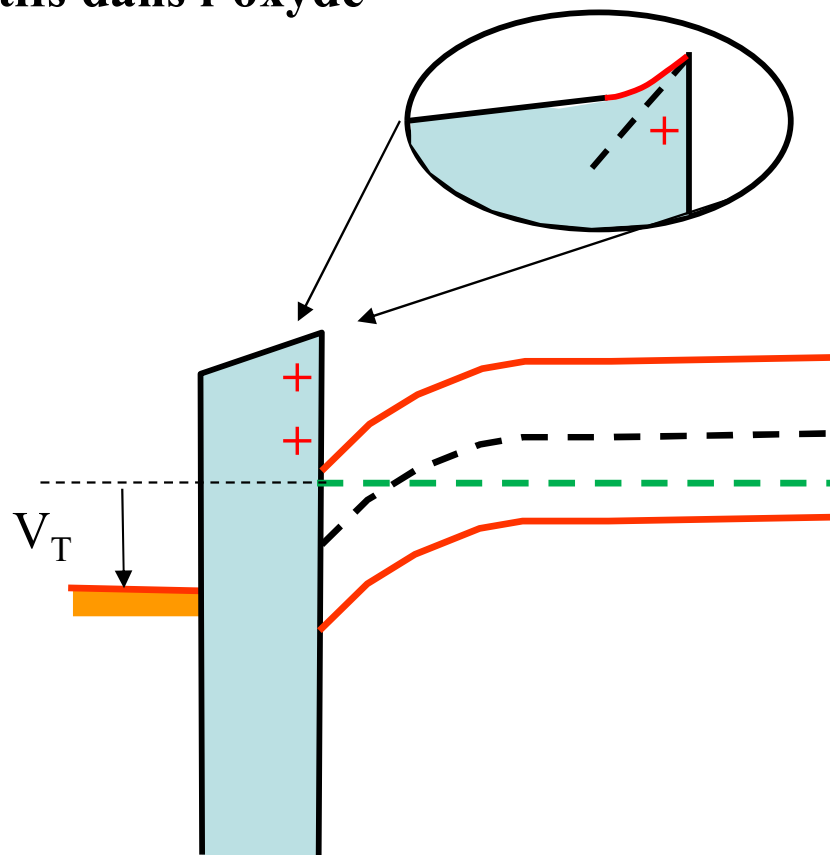
Après introduction de charges fixes positives à l'interface:

	Augmente	Diminue	Reste fixe
Potentiel de surface ψ_s			
Charges d'espace dans la zone de déplétion			
Champ électrique dans l'oxyde			
Charges dans le métal			
Tension électrique sur le métal (Tension de threshold V_T)			

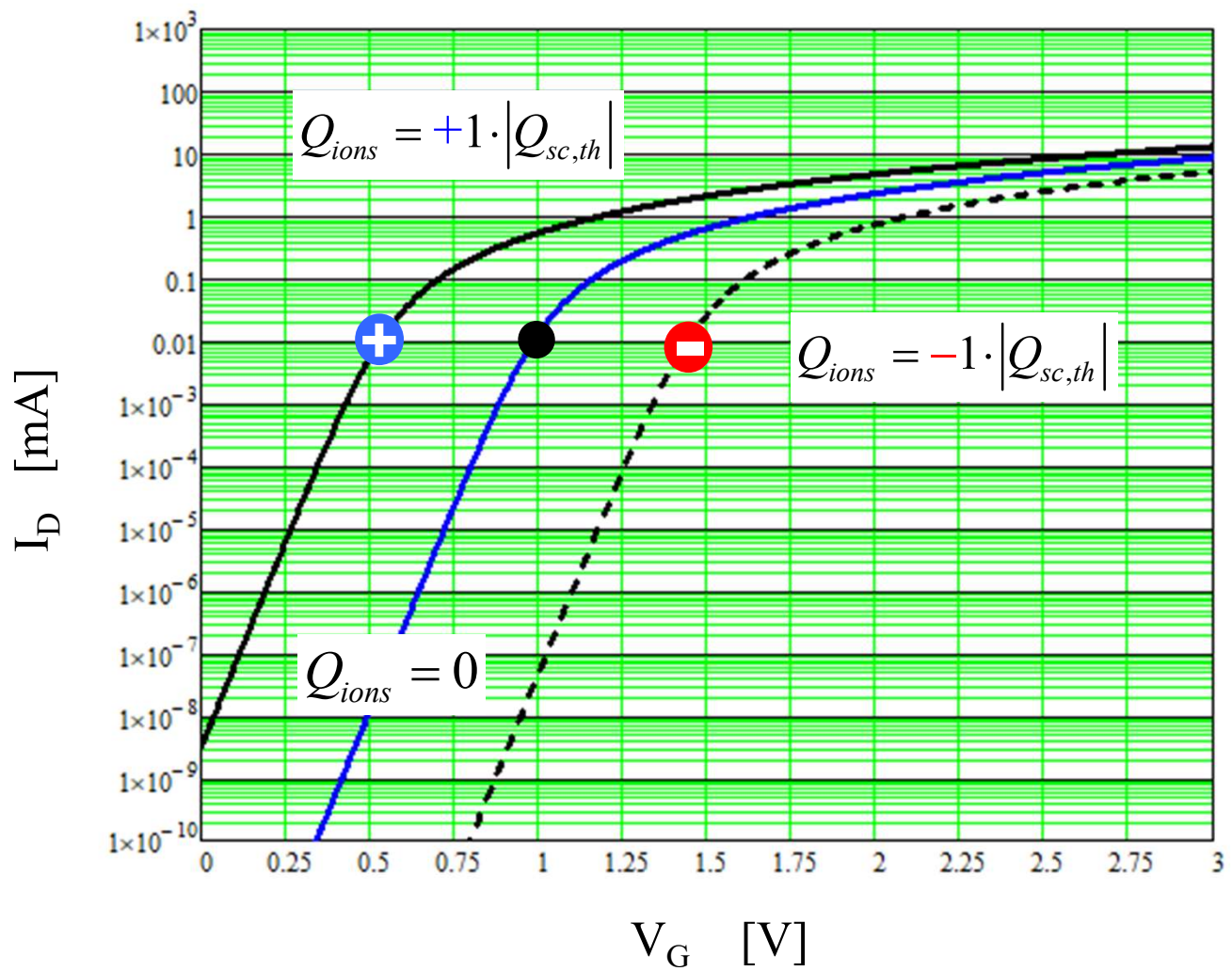
Situation de depart sans ion dans l'oxyde



Ions positifs dans l'oxyde



Réduction du threshold



$$N_A = 10^{17} \text{ cm}^{-3}$$

$$\epsilon_{ox} = 4$$

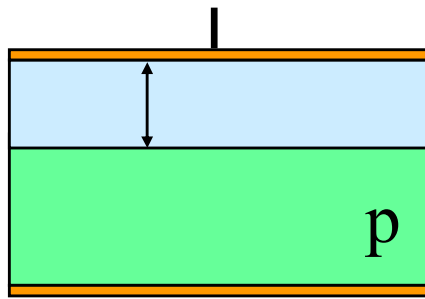
$$d_{ox} = 10 \text{ nm}$$

$$|Q_{sc,th}| = 1.6 \cdot 10^{-15} \left[C / \mu m^2 \right]$$

$$n = 1.27 \quad \text{dans les trois cas}$$

$$V_T = V_{T0} - \frac{Q_{ion}}{C_{ox}}$$

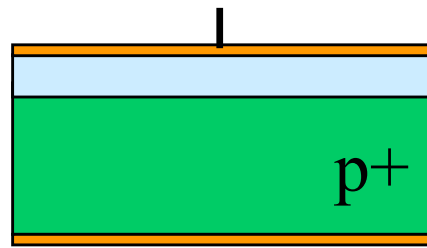
Field Oxide



d_{ox} ↗

V_T ↗

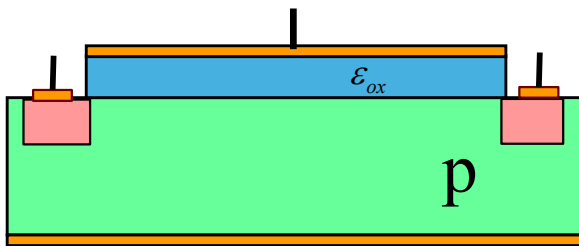
Channel stop



p ↗

V_T ↗

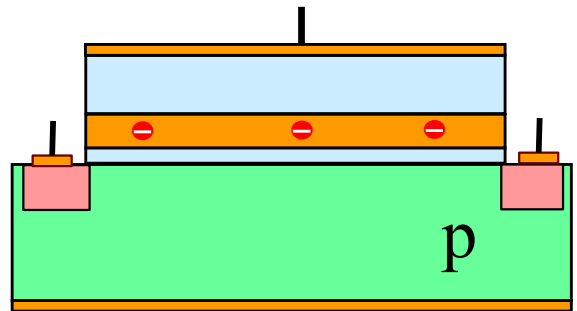
High K



ϵ_{ox} ↗

V_T ↘

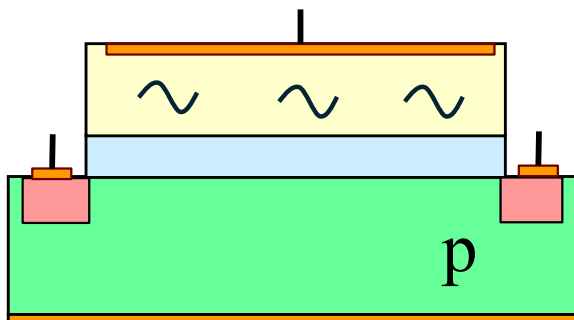
Floatging gate memory



⊖ ↗

V_T ↗

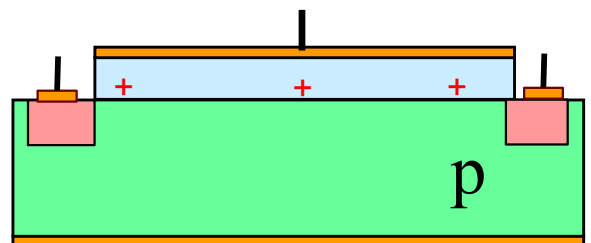
ISFET



~ - V_T ↗

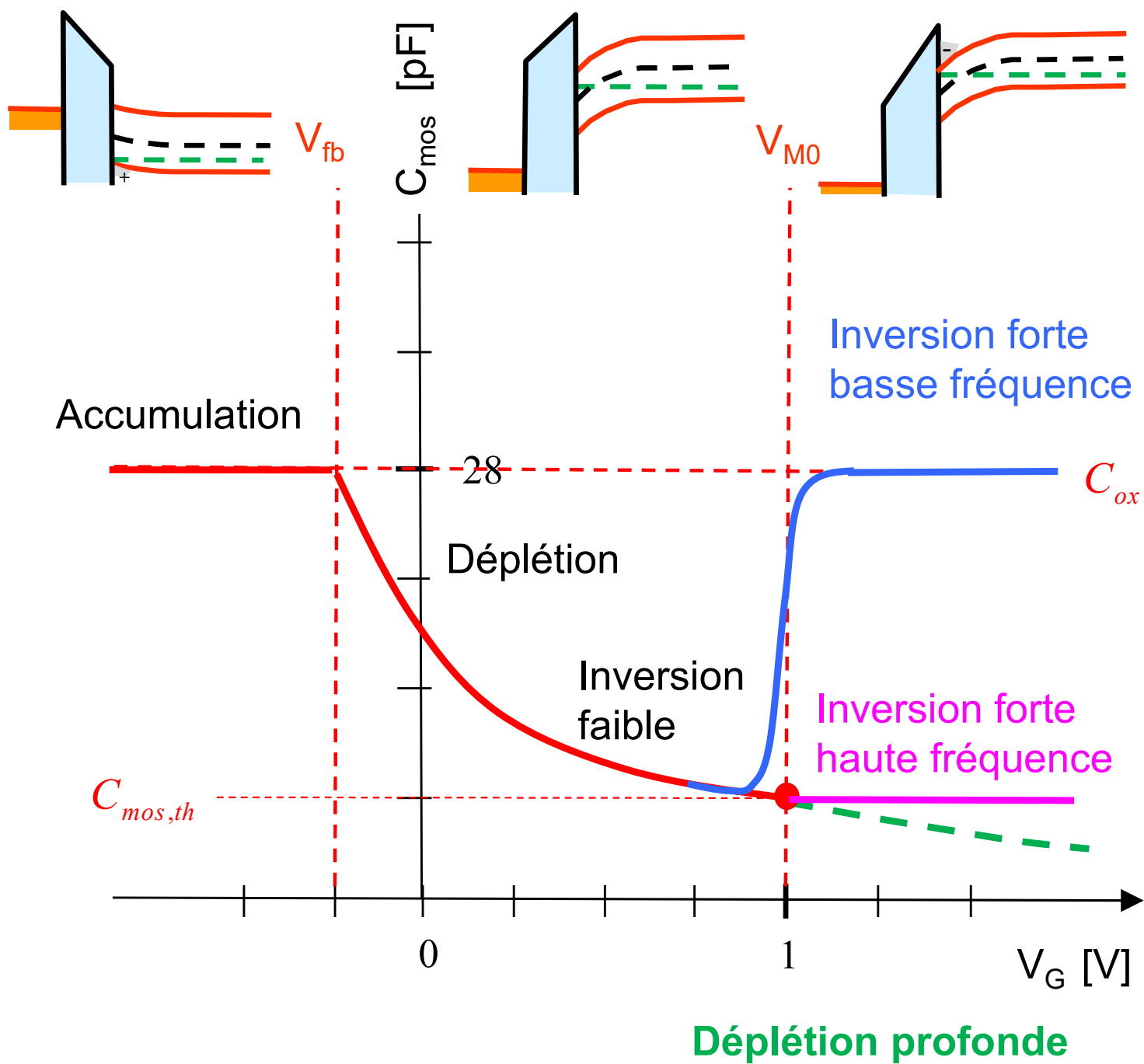
~ + V_T ↘

Ion implant



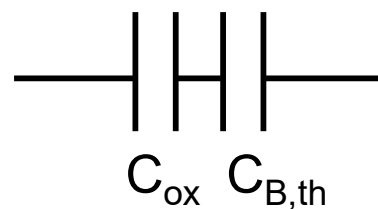
+ V_T ↘

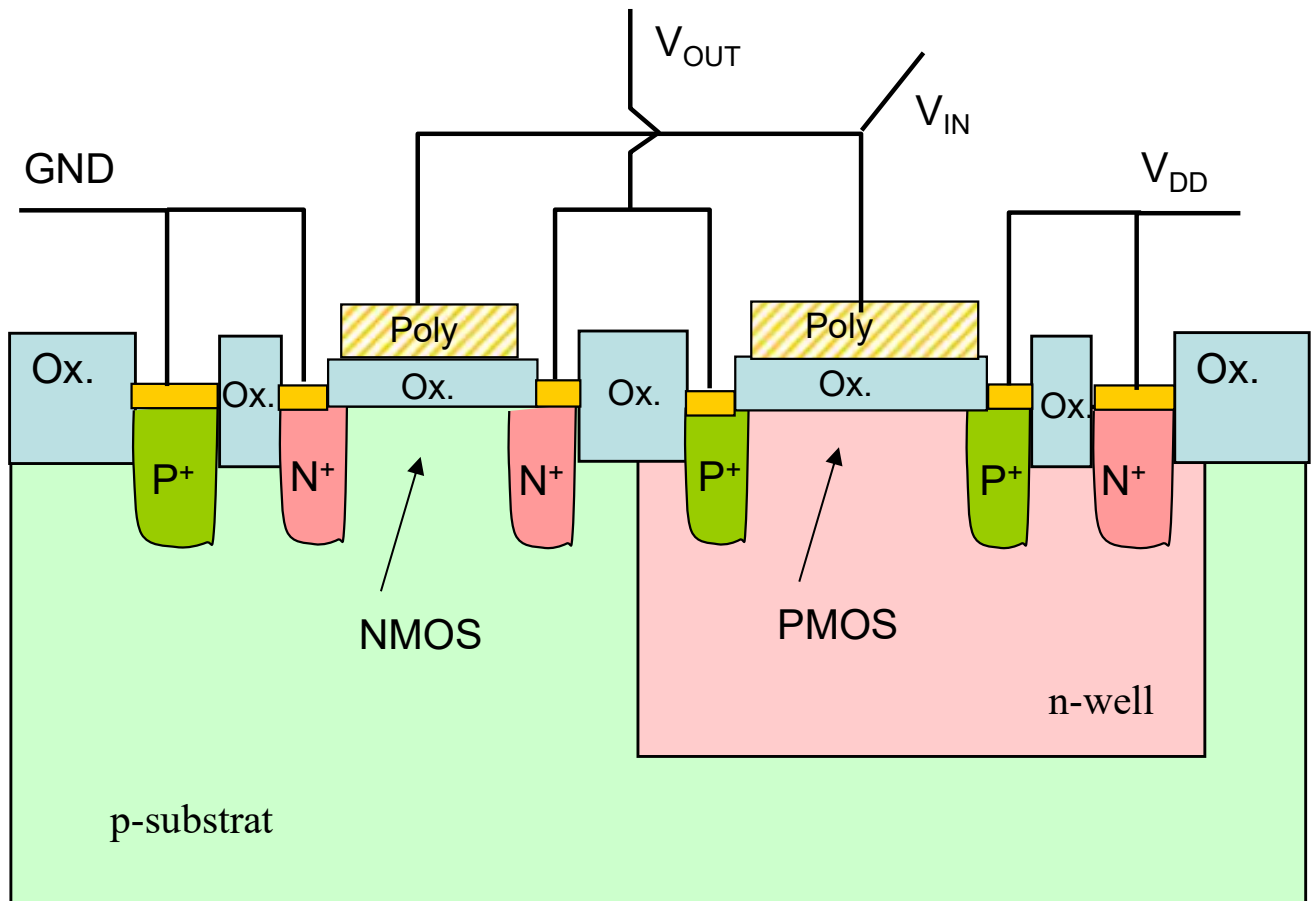
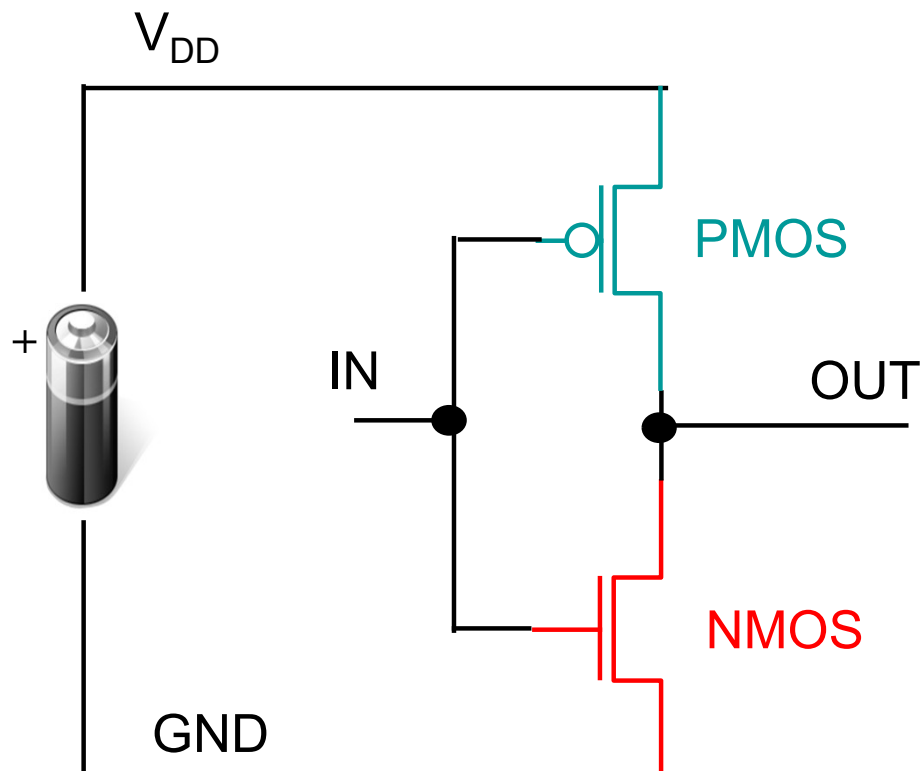
- V_T ↗

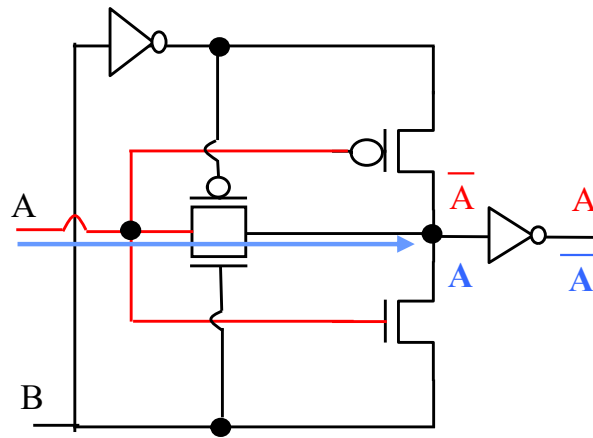


$$C_{mos,th} = \frac{C_{ox} \cdot C_{B,th}}{C_{ox} + C_{B,th}} = C_{ox} \cdot \frac{C_{B,th} / C_{ox}}{1 + C_{B,th} / C_{ox}}$$

$$C_{mos,th} = C_{ox} \cdot \frac{n-1}{n} = 7 [pF]$$







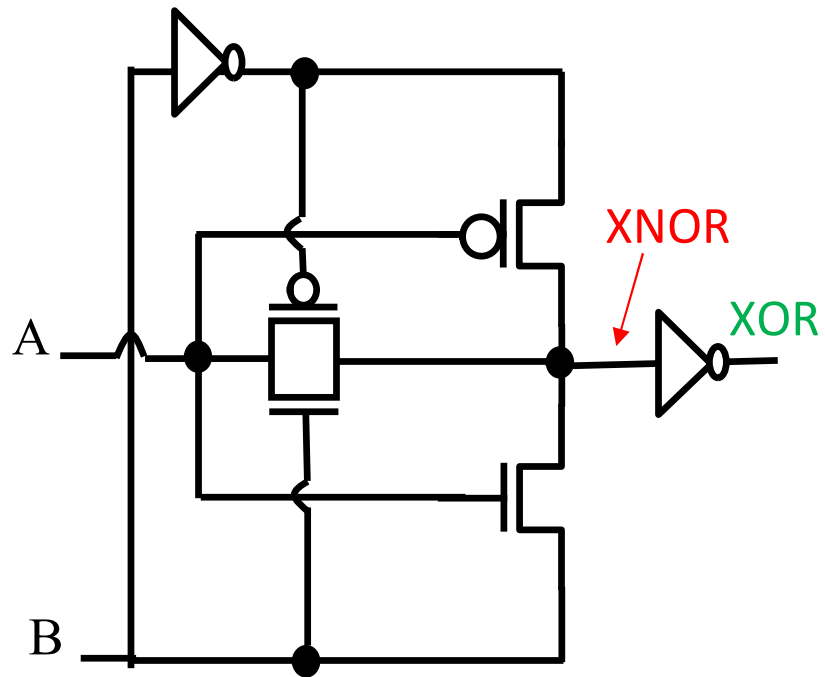
XOR avec 8 transistors

(voir script)

L'inverseur final sert à isoler la sortie de l'entrée !

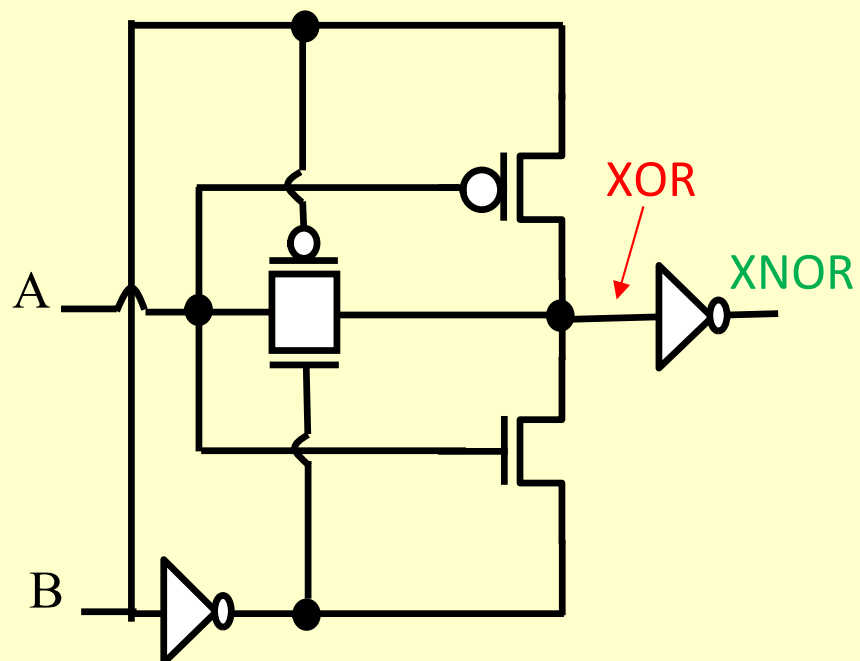
A	B		OUT
0	0	1	0
1	0	0	1
0	1	0	1
1	1	1	0

XNOR XOR



XOR: 8 transistors et isolation

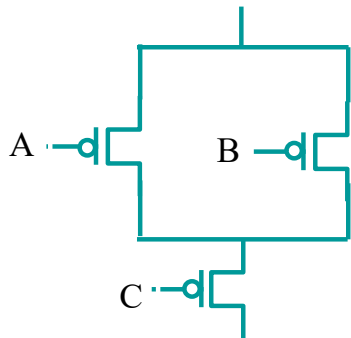
XNOR: 6 transistors sans isolation



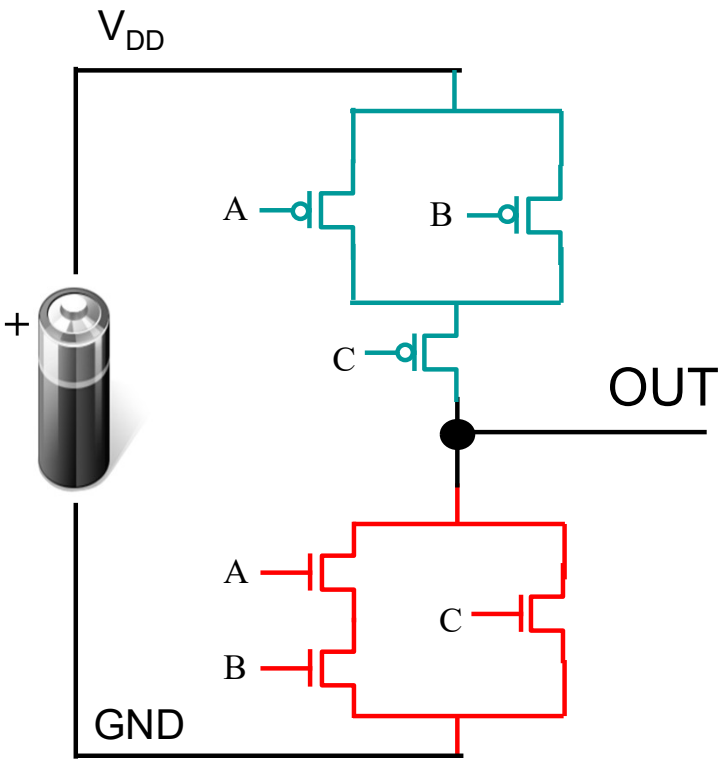
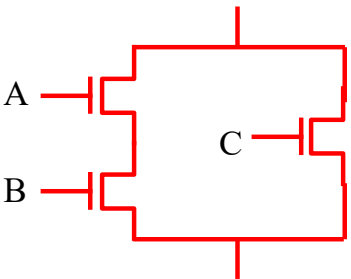
XNOR: 8 transistors et isolation

XOR: 6 transistors sans isolation

PMOS



NMOS



(voir script) AOI-21 $\rightarrow$ $[(A \text{ et } B) \text{ ou } C]$

And-Or-Invert

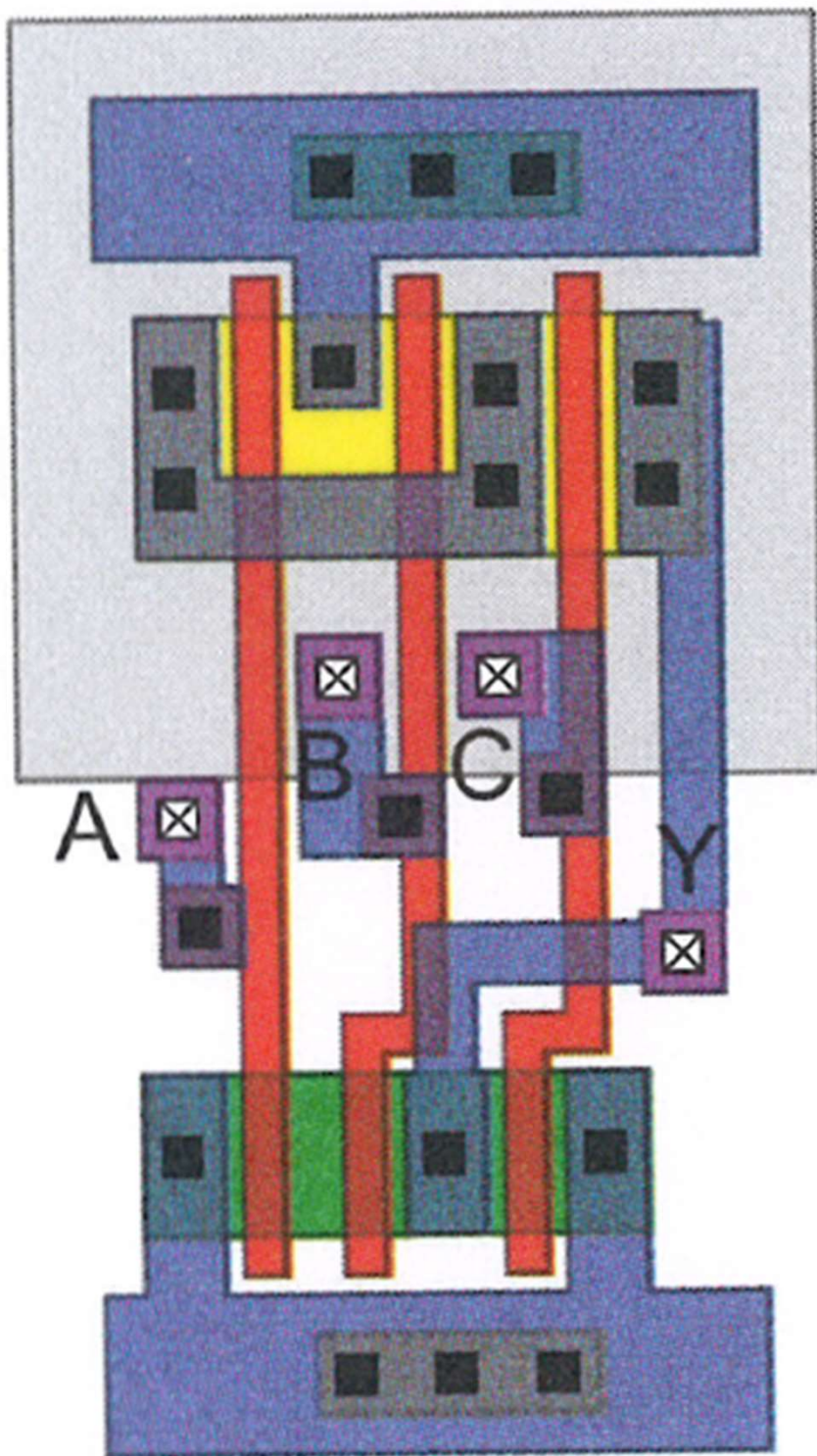
OR

AND

A	B	C	AOI-21
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Layout AOI-21

«And-Or-Invert»



Weste/Harris, « CMOS VLSI design », Addison-Wesley